In re DAVID GLEN ROE, Application No. 09/814,244
Amendment D

Amendment to the Claims:

The listing of clams will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (currently amended): ~~A circuit~~ An application-specific integrated circuit (ASIC) comprising:

a first phase-locked loop circuit including: an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, ~~and~~ a buffered reference clock output, and a buffer electrically connected to the off-chip reference clock input and the buffered reference clock output, and wherein the first phase-locked loop circuit is defined in one or more predefined libraries of circuits; and

a second phase-locked loop circuit including: an on-chip reference clock input and a second set of one or more phase-locked loop clock outputs, wherein the second phase-locked loop circuit is defined in said one or more predefined libraries of circuits and is specified to be connected to an output of a receiver on the ASIC;

wherein the buffered reference clock output of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit.

2 (currently amended): The ~~circuit~~ ASIC of claim 1, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit includes at least two phase-locked loop clock outputs.

3-7 (canceled)

8 (currently amended): The ~~circuit~~ ASIC of claim 1, wherein the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad of a chip.

9 (currently amended): ~~A circuit~~ An application-specific integrated circuit (ASIC) for receiving an external clock input to generate a first internal clock signal and a second internal clock signal, the ~~circuit~~ ASIC comprising:

a first phase-locked loop circuit means including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, a buffered reference clock output, and means for buffering a received off-chip reference clock signal electrically coupled ~~between~~ to the off-chip reference clock input and the buffered reference clock output, wherein the first phase-locked loop circuit means is defined in one or more predefined libraries of circuits; and

a second phase-locked loop circuit means including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs, wherein the second phase-locked loop circuit means is defined in said one or more predefined libraries of circuits and is specified to be connected to an output of a receiver on the ASIC;

wherein the buffered reference clock output of the first phase-locked loop circuit means is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit means.

10 (currently amended): The ~~circuit~~ ASIC of claim 9, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit means includes at least two phase-locked loop clock outputs.

11-13 (canceled)

14 (currently amended): The ~~circuit~~ ASIC of claim 9, wherein the off-chip reference clock input of the first phase-locked loop circuit means is directly electrically coupled to a pad of a chip.

15-20 (canceled)